

# Reference Schematic For RK1808

**RK1808\_EDGE\_COMPUTING\_REF\_V10**

PMIC: RK809-2 (5BUCK + 9LDO + Codec)  
RAM: DDR3/L /LPDDR3  
ROM: eMMC/SPI NOR + TF card  
Interface: MIPI CSI/MIPI DSI/UART/SPI/CIF/BT1120/PCIE/USB3/Micro-SD

**Rockchip Confidential**

 瑞芯微电子		Fuzhou Rockchip Electronics		
Project:	RK1808_REF_V10			
File:	00.Cover Page			
Date:	Thursday, January 03, 2019		Rev:	V1.0
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## Note

### NOTE 1:

#### Component parameter description

1. DNP stands for component not mounted temporarily
2. If Value or option is DNP, which means the area is reserved without being mounted
3. If Flash is compatible, please notice when eMMC is used, the option is that @eMMC is mounted, @Nand is not mounted when Nand is used, the option is that @Nand is mounted, @eMMC is not mounted

### NOTE 2:

Please use our recommended components to avoid too many changes.For more informations about the second source,please refer to our AVL.

Note

Option

Description

Remind

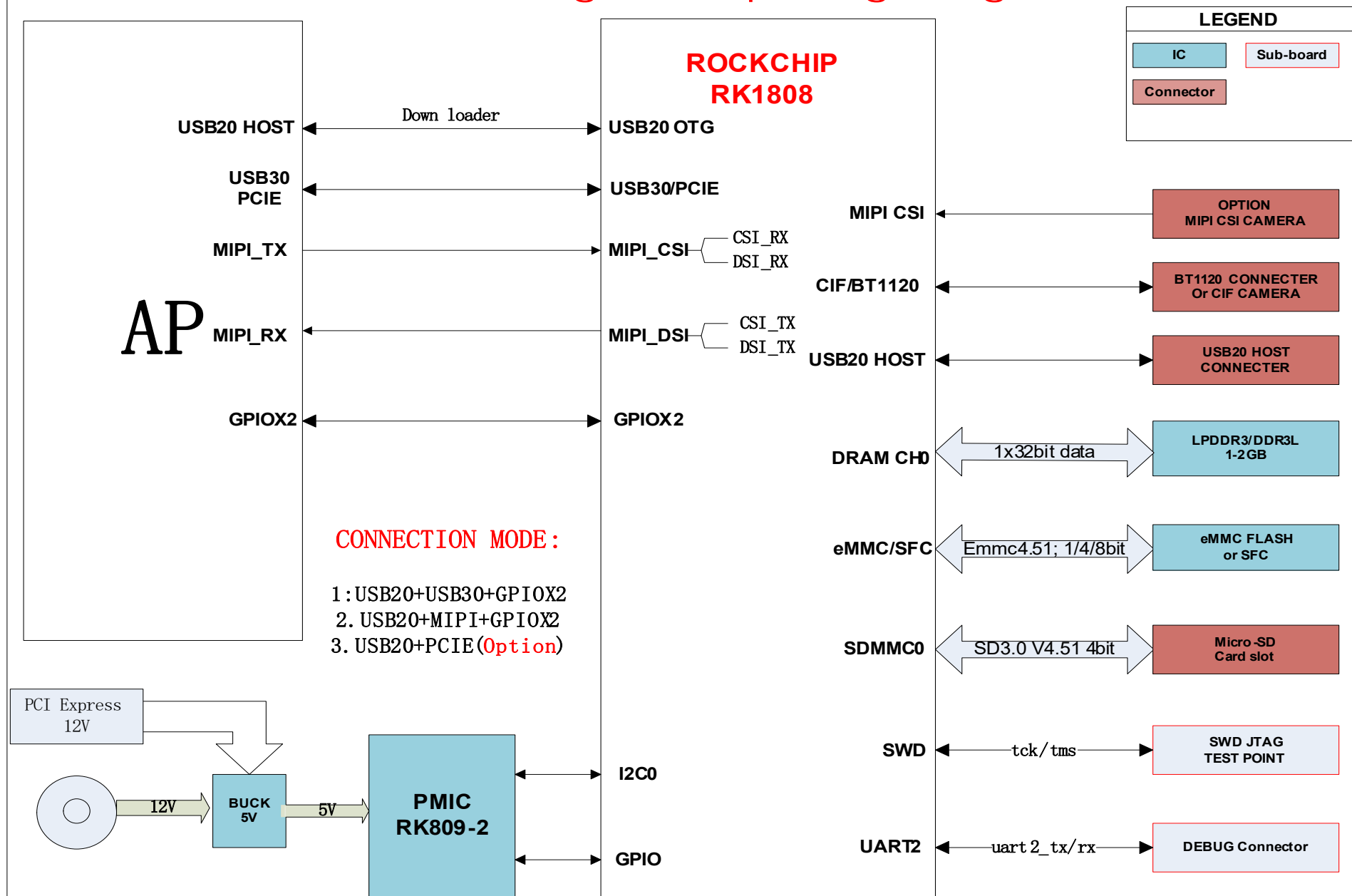


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# RK1808 Edge Computing Diagram




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Project:	RK1808_REF_V10		
File:	03.Block Diagram		
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I2C MAP

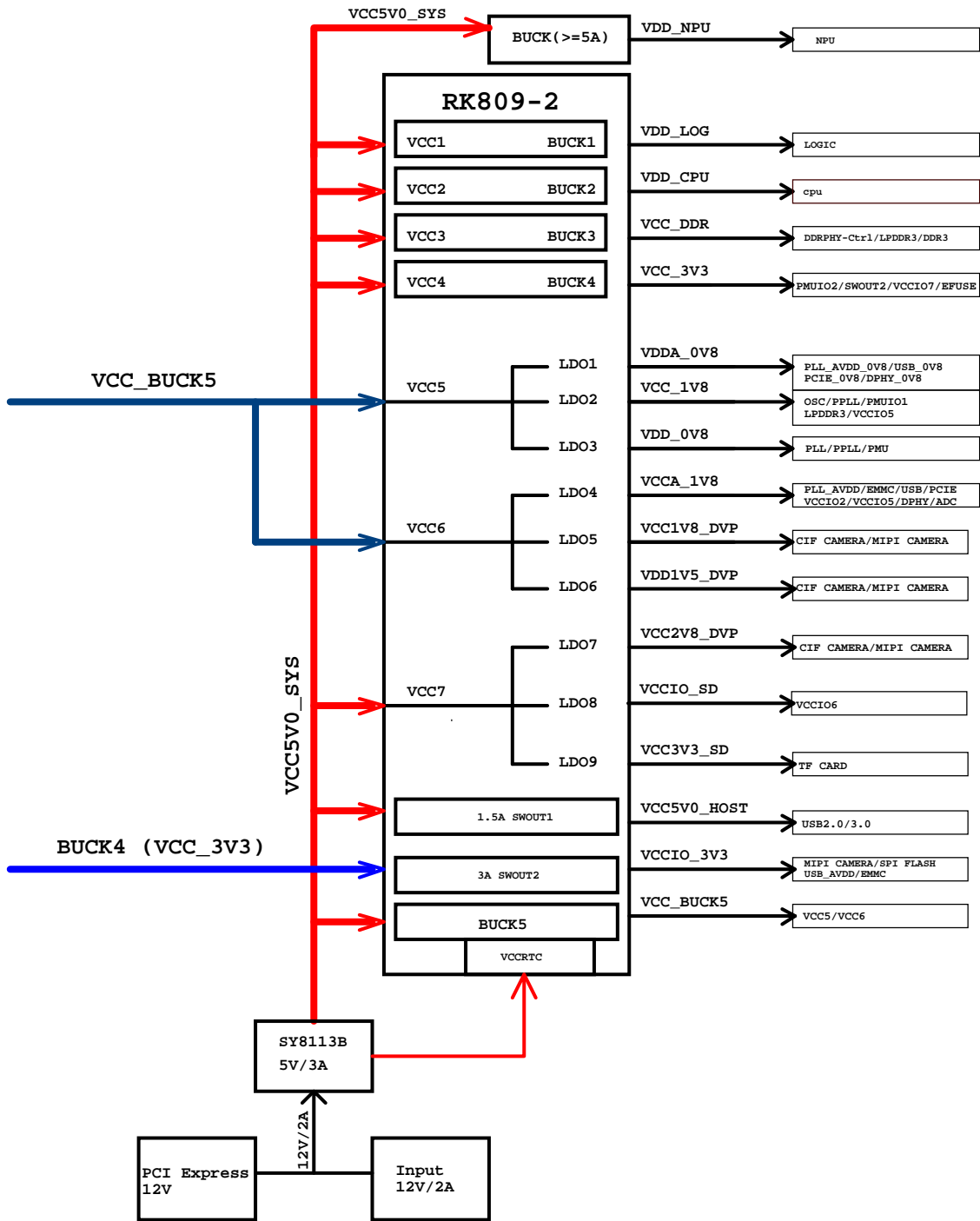
Port	Pin name	Domain	Bus name	Pull-up voltage	Slave Device	Slave Addr (MS 7Bits)	Note	Slave Bus Capability
I2C0	I2C0_SCL_u I2C0_SDA_u	PMUIO2	I2C0_SCL_PMIC I2C0_SDA_PMIC	VCC_3V3	Rockchip RK809	0x20	PMIC	100kHz, 400kHz
					TCS4525	0X1C	BUCK	100kHz, 400kHz
I2C3	I2C3_SCL_u I2C3_SDA_u				OV5695 GC2145	0X36 0X3C	MIPI CAMERA CIF CAMERA	100kHz, 400kHz
I2C4	I2C4_SCL_u I2C4_SDA_u	VCC_3V3		VCC_3V3			PCIE	100kHz, 400kHz



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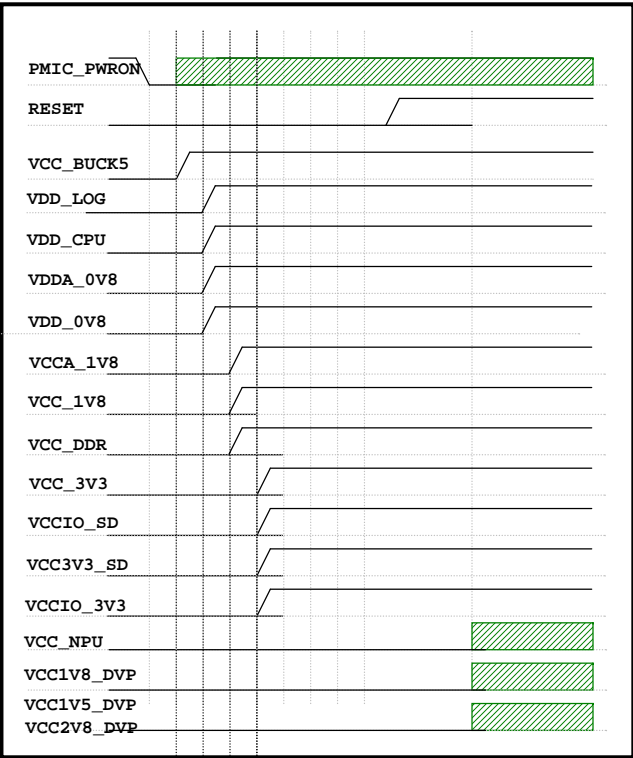
Project:	RK1808_REF_V10		
File:	04.I2C MAP		
Date:	Thursday, January 03, 2019	Rev:	V1.0
Designed by:	Rzf	Sheet:	4 of 98

POWER DIAGRAM

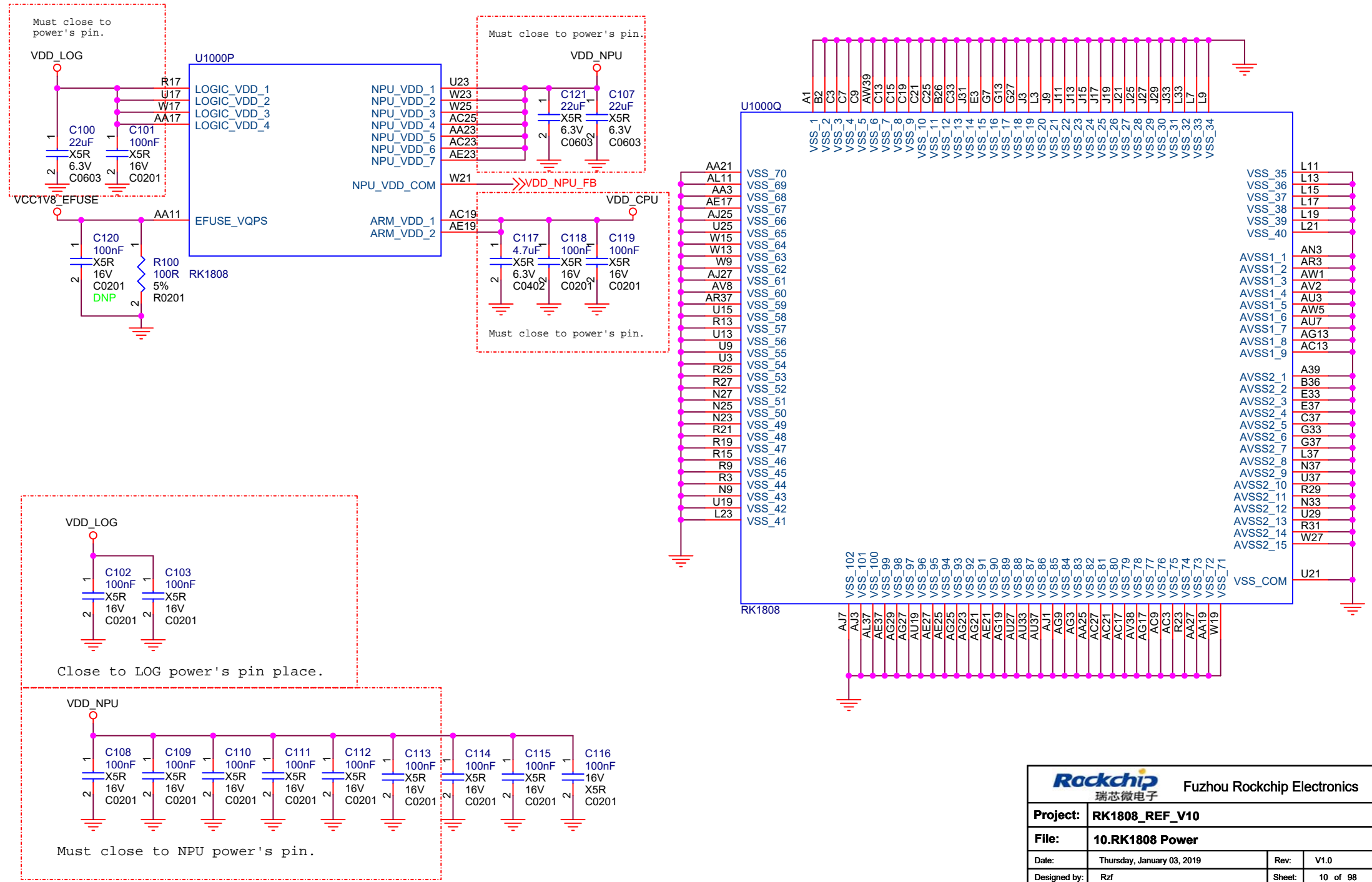


RK809-2 Power-on Sequence

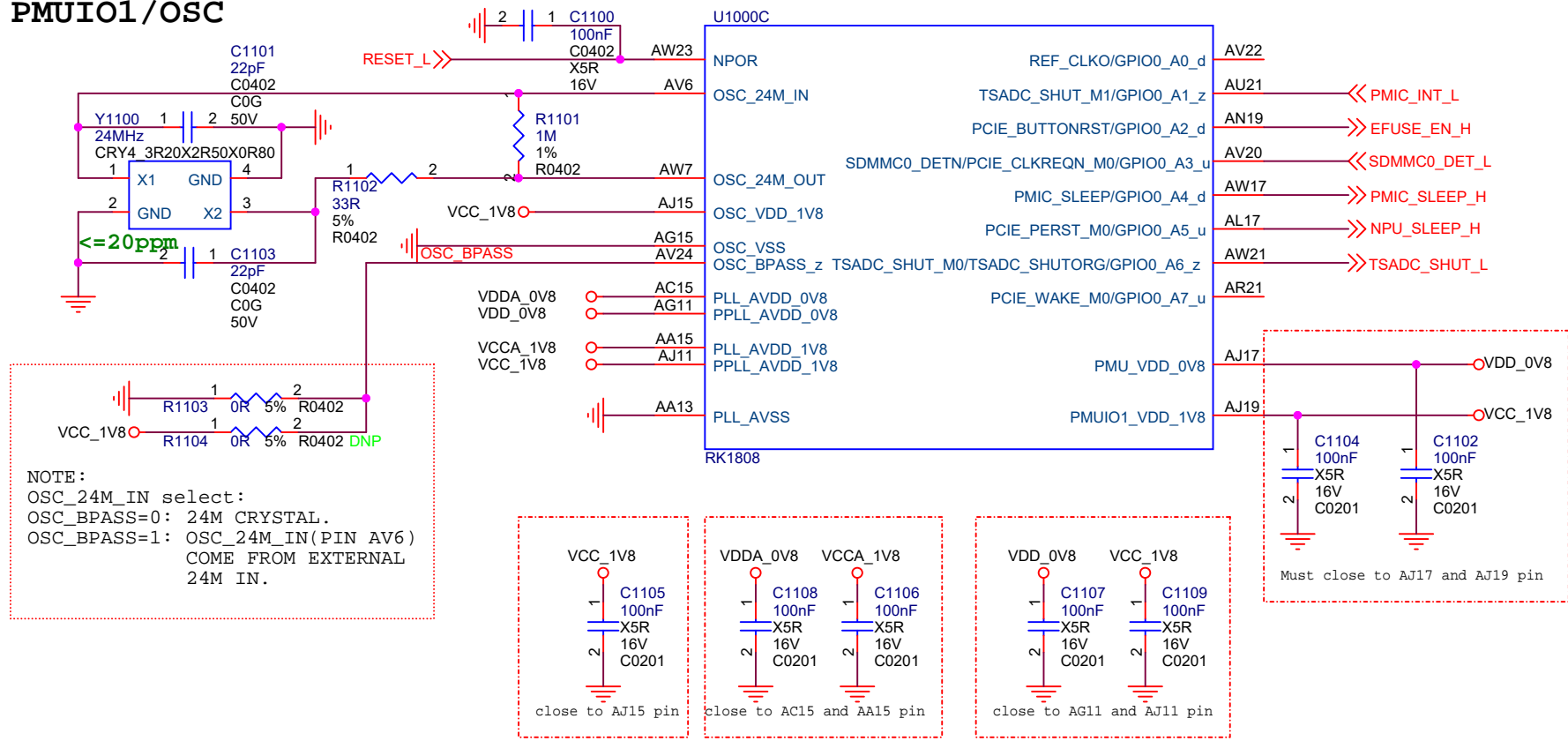
PowerName	PMIC Channel	Time Slot (step 2mS)	Default voltage	Supply Limit	Default ON/OFF	Sleep ON/OFF	Peak Current
VDD_NPU	EXTERNAL(>=5A)		1.05V	6A	OFF	OFF	4A
VDD_LOG	BUCK1	Slot:2	0.85V	2.5A	ON	OFF	1.25A
VDD_CPU	BUCK2	Slot:2	0.85V	2.5A	ON	OFF	750ma
VCC_DDR	BUCK3	Slot:3	FB=0.6V	1.5A	ON	ON	
VCC_3V3	BUCK4	Slot:4	3.3V	1.5A	ON	ON	
VCC_BUCK5	BUCK5	Slot:1	2.5V	2.5A	ON	ON	
VDDA_0V8	LD01	Slot:2	0.8V	400mA	ON	OFF	
VCC_1V8	LD02	Slot:3	1.8V	400mA	ON	ON	
VDD_0V8	LD03	Slot:2	0.8V	100mA	ON	ON	
VCCA_1V8	LD04	Slot:3	1.8V	400mA	ON	OFF	
VCC1V8_DVP	LD05		1.8V	400mA	OFF	OFF	
VDD1V5_DVP	LD06		1.5V	400mA	OFF	OFF	
VCC2V8_DVP	LD07		2.8V	400mA	OFF	OFF	
VCCIO_SD	LD08	Slot:4	3.3V	400mA	ON	OFF	
VCC3V3_SD	LD09	Slot:4	3.3V	400mA	ON	OFF	
VCCIO_3V3	SWOUT2	Slot:4	3.3V	2A	ON	OFF	
VCC5V0_HOST	SWOUT1		5V	1.5A	OFF	OFF	
RESET	RESETB	Slot:10	OD				



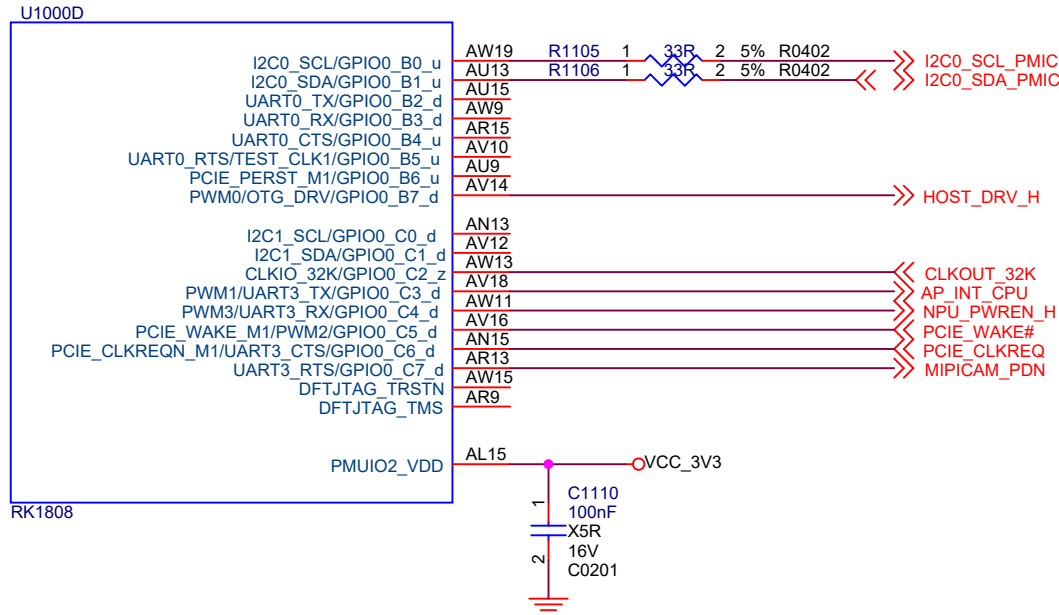
## RK1808 Power




## PMUIO1/OSC



## PMUIO2



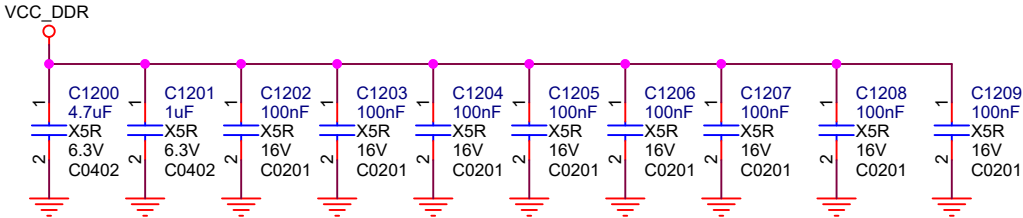
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Project:	RK1808_REF_V10
File:	11.RK1808 OSC/PMUIO1/PMUIO2
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DDR Controller



LPDDR3/LPDDR2	DDR3
A0	A9
A1	A14
A2	A13
A3	A11
A4	A2
A5	A4
A6	A3
A7	A6
A8	A5
A9	A1
	A0
	A7
	CASB
	A8
	ODT0
	BA1
	RASB
	CSB0
	BA2
	A12
	BA0
	WEB
CK	CK
CKB	CKB
CKE	CKE
CSB0	A10
CSB1	CSB1
ODT0	A15
ODT1	ODT1
	RESETN





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Project:	RK1808_REF_V10		
File:	12.RK1808 DDR Controller		
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The diagram shows a circuit for connecting VCCIO\_EMMC to two different voltage levels. A purple line from VCCIO\_EMMC splits into two paths. The top path goes through a resistor labeled R1300 (with a '1' above it), a blue zigzag line representing a 5% tolerance, and another resistor labeled R0402 (with a '2' above it) to a red circle labeled VCCA\_1V8. The bottom path goes through a resistor labeled R1301 (with a '1' above it), a blue zigzag line representing a 5% tolerance, and another resistor labeled R0402 (with a '2' above it) to a red circle labeled VCCIO\_3V3. The word 'DNP' is written in green next to the R0402 resistor in the bottom path.

NOTE:  
Select vccio0 voltage according to different flash.

U1000G

RK1808

SPI0\_MOSI/I2C2\_SCL\_M1/UART1\_RX\_M1/GPIO1\_B4\_u  
 SPI0\_MISO/I2C2\_SDA\_M1/UART1\_TX\_M1/GPIO1\_B5\_u  
 SPI0\_CSN/PWM4/GPIO1\_B6\_u  
 SPI0\_CLK/PWM5/GPIO1\_B7\_d


VCCIO5

C27  
 A27  
 G25  
 E25  
 L25

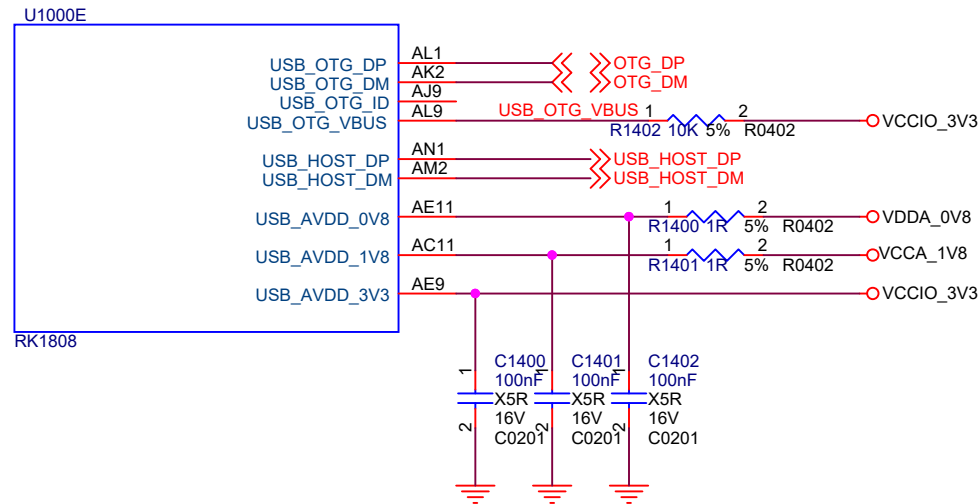
VCC\_1V8

C1301  
 100nF  
 X5R  
 16V  
 C0201

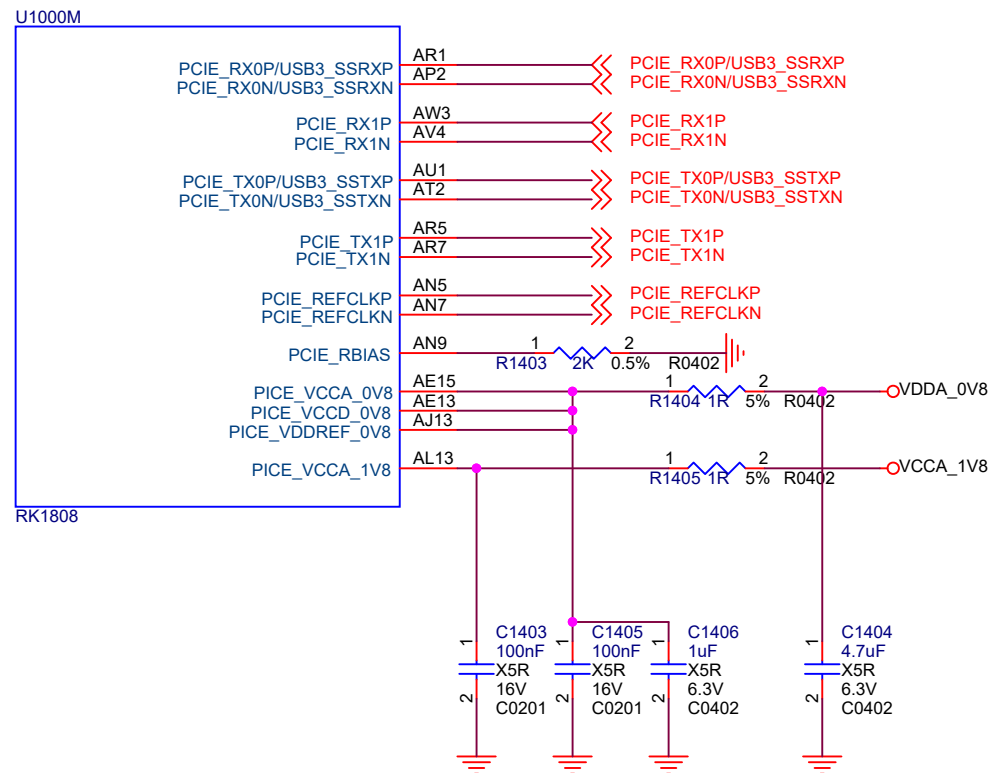
Note:  
 VCCIO5 must be powered,  
 SPI0\_CSN (Pin G25) must  
 keep pull-up during start-up.


 <div style="display: inline-block; vertical-align: middle; margin-left: 10px;"> <b>Fuzhou Rockchip Electronics</b>              瑞芯微电子         </div>			
<b>Project:</b>	<b>RK1808_REF_V10</b>		
<b>File:</b>	<b>13.RK1808 EMMC /SPI0 Controller</b>		
<b>Date:</b>	Thursday, January 03, 2019	<b>Rev:</b>	V1.0
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## USB Controller

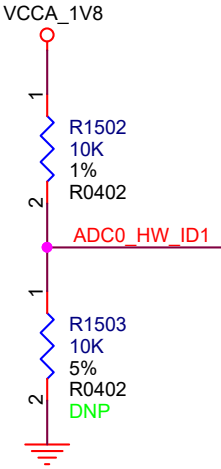
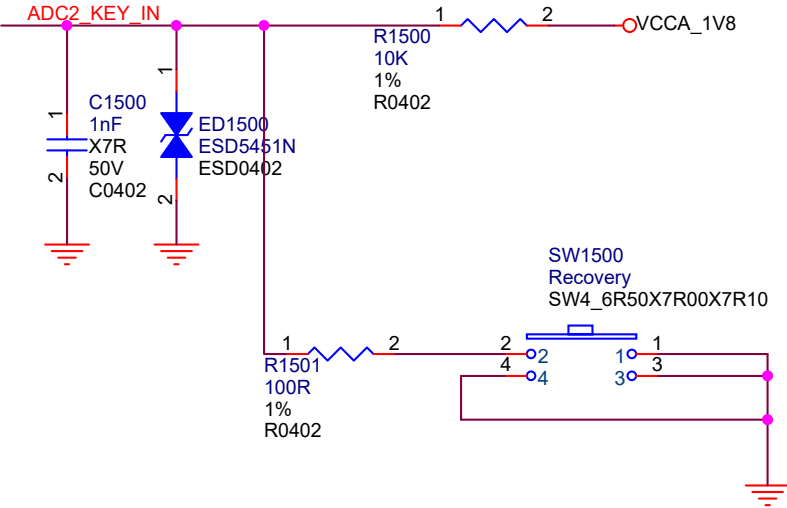
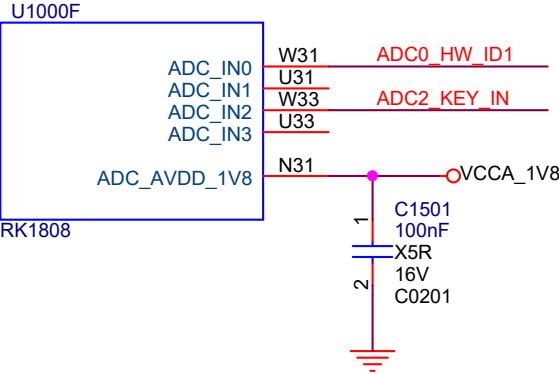


## PCIE Controller




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File:	14.RK1808 USB/PCIE Controller		
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SARADC



Rev	Vadc	Stuff
V10	1.8V	R1502=10K,R1503=NC
V20	0.9V	R1502=R1503=10K
V30	0V	R1502=NC,R1503=10K



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Project:

RK1808\_REF\_V10

File:

15.RK1808 SARADC

Date:

Thursday, January 03, 2019

Rev:

V1.0

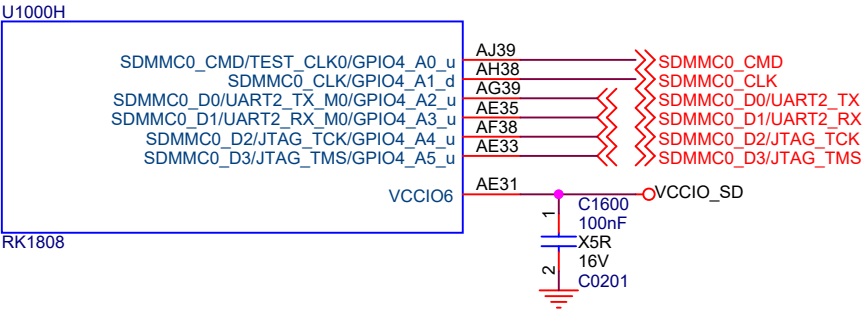
Designed by:

Rzf

Sheet:

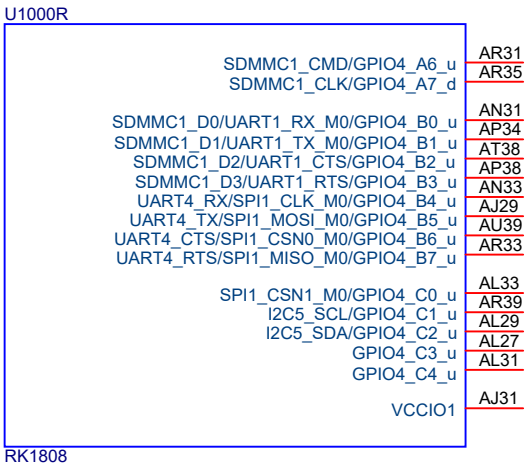
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SDMMC0 Controller

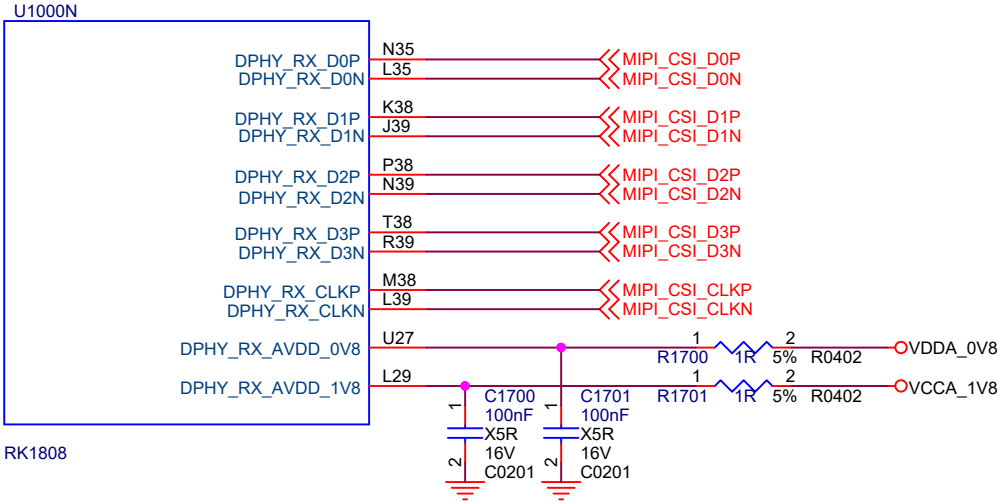


→ For Micro-SD(TF) card

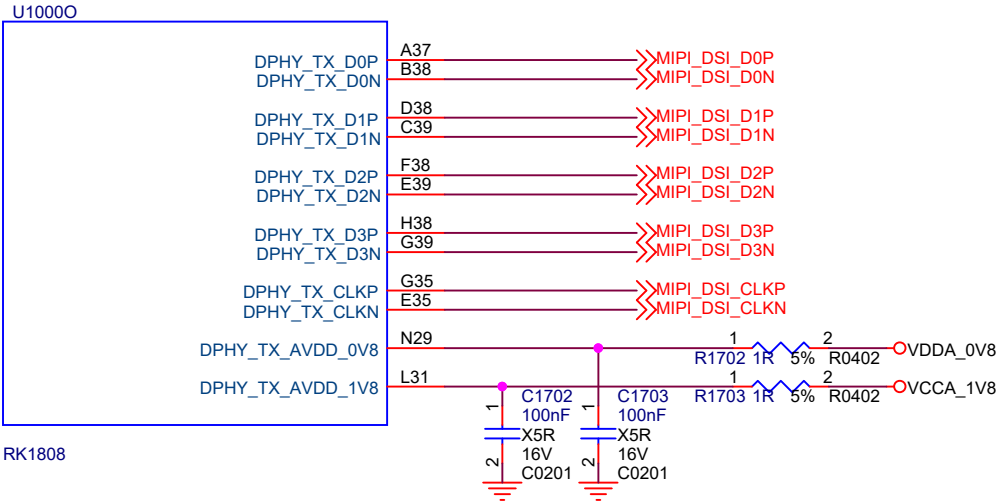
SDMMC1 Controller




MIPI CSI Controller

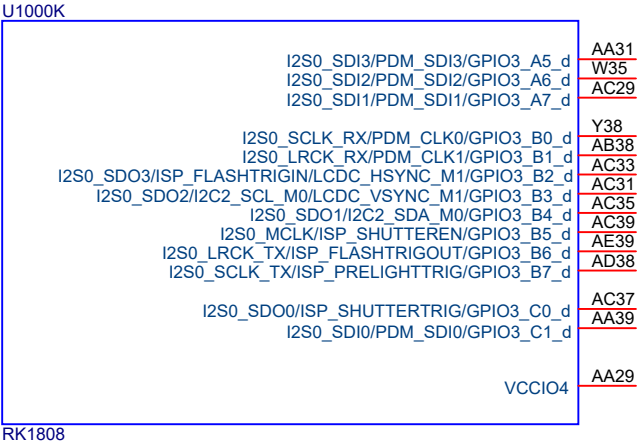


MIPI DSI Controller

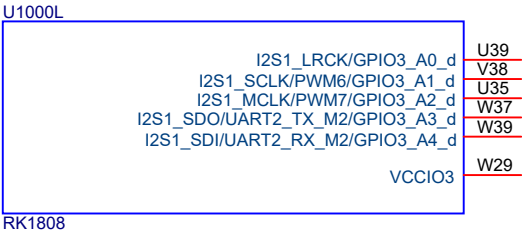


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Project:	RK1808_REF_V10		
File:	17.RK1808 MIPI DSI/CSI		
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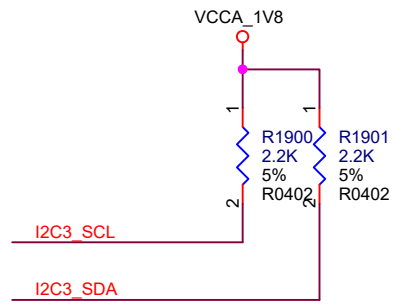
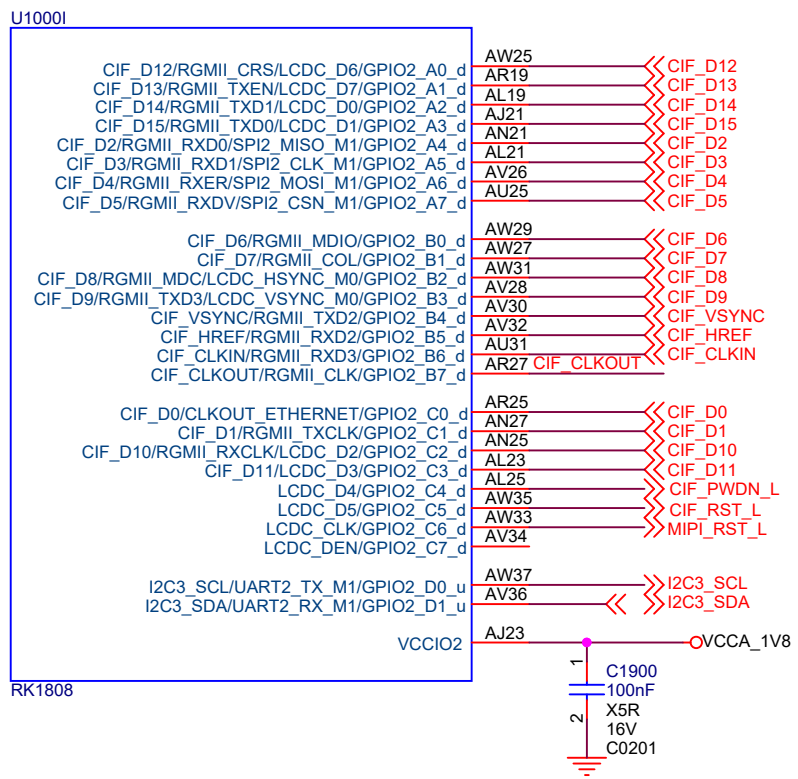
I2S0 Controller



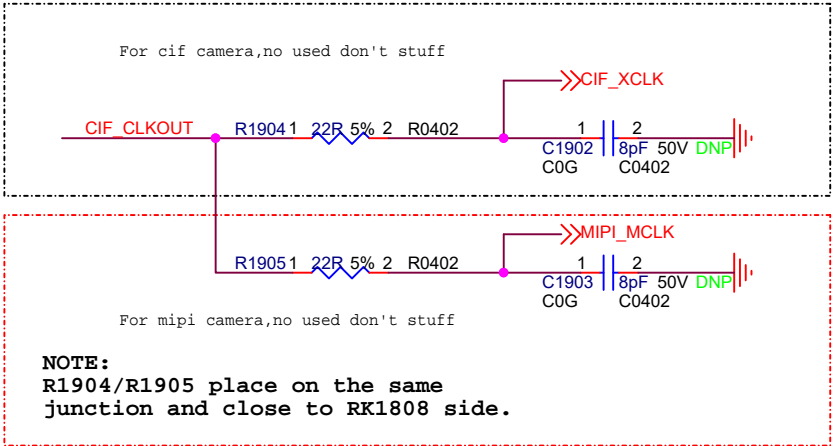
I2S1 Controller



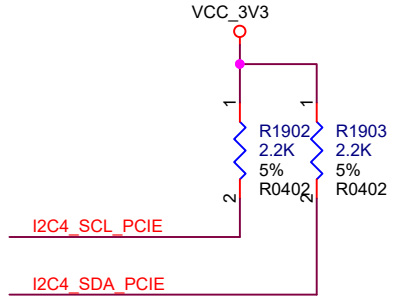
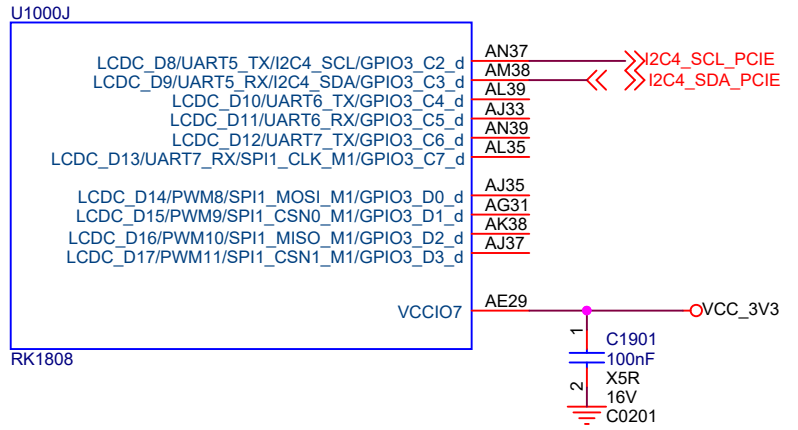
CIF/RGMII/LCDC Controller




**NOTE:**  
RGMII\CIF\LCDC\GPIO: Only used one function at the same time



LCDC Controller





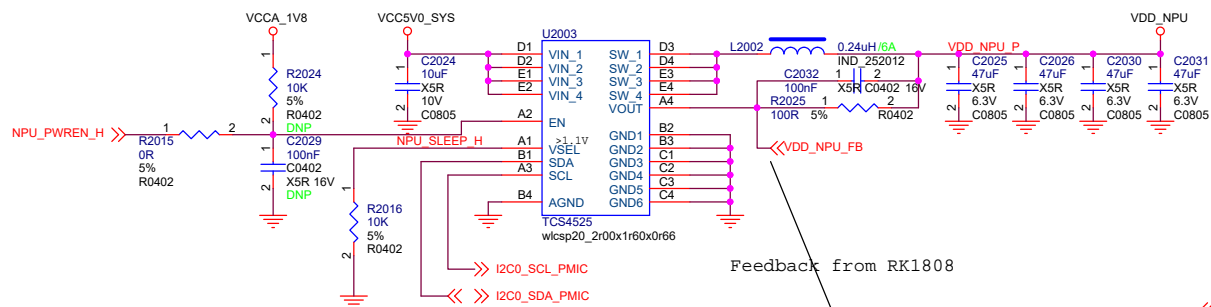
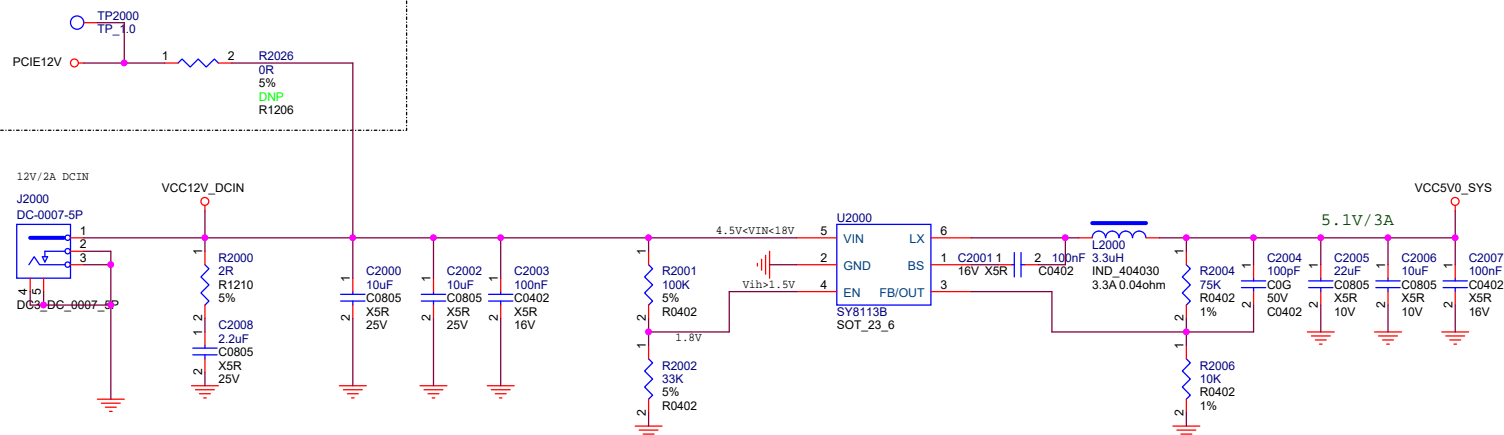
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Project:	RK1808_REF_V10		
File:	19.RK1808 RGMII/LCDC/CIF/BT1120		
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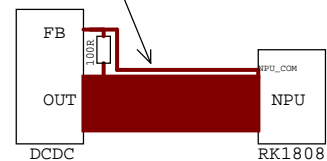
# DC IN&SYSTEM Power

RK1808 is PCI Express add in card(EP), power come from RC device.

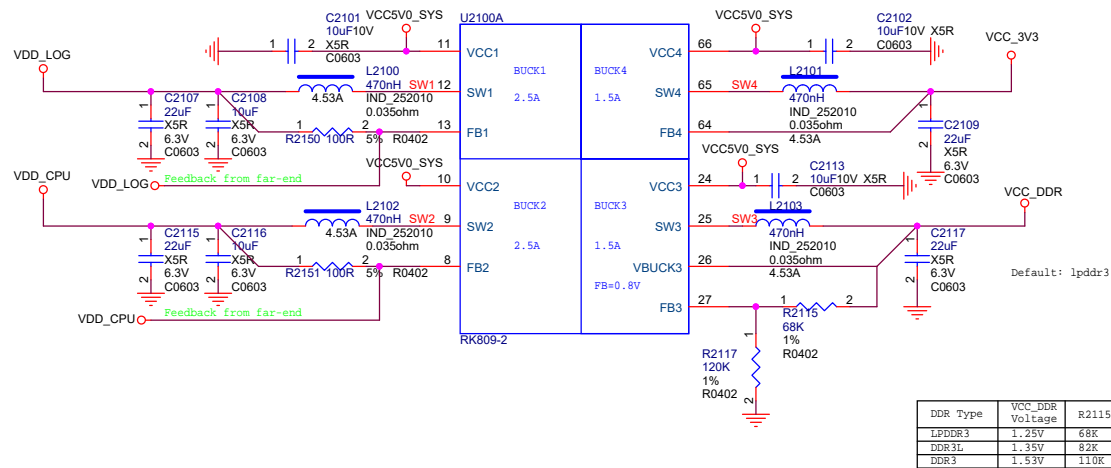


NOTE:  
VDD\_NPU: Imin>=5A, Ripple<=80mV

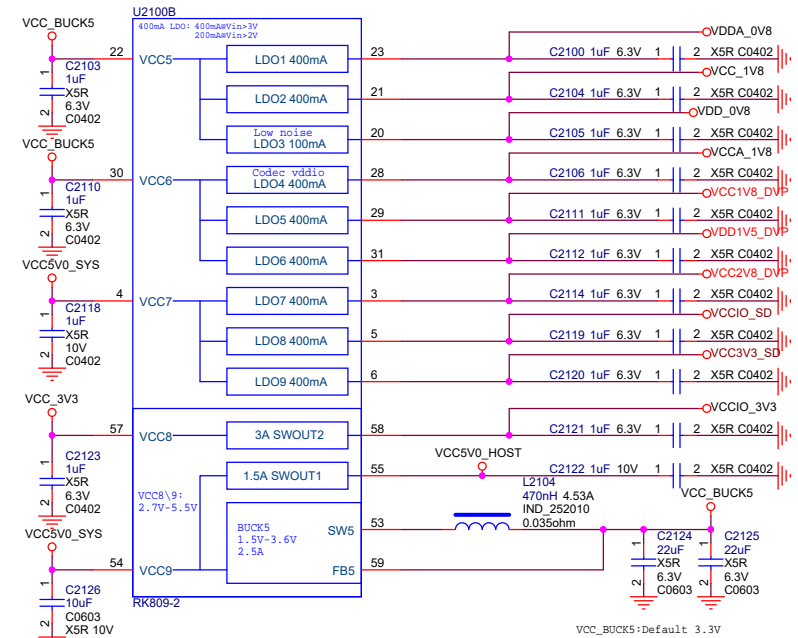
Feedback from RK1808



## PMIC RK809-2 DCDC

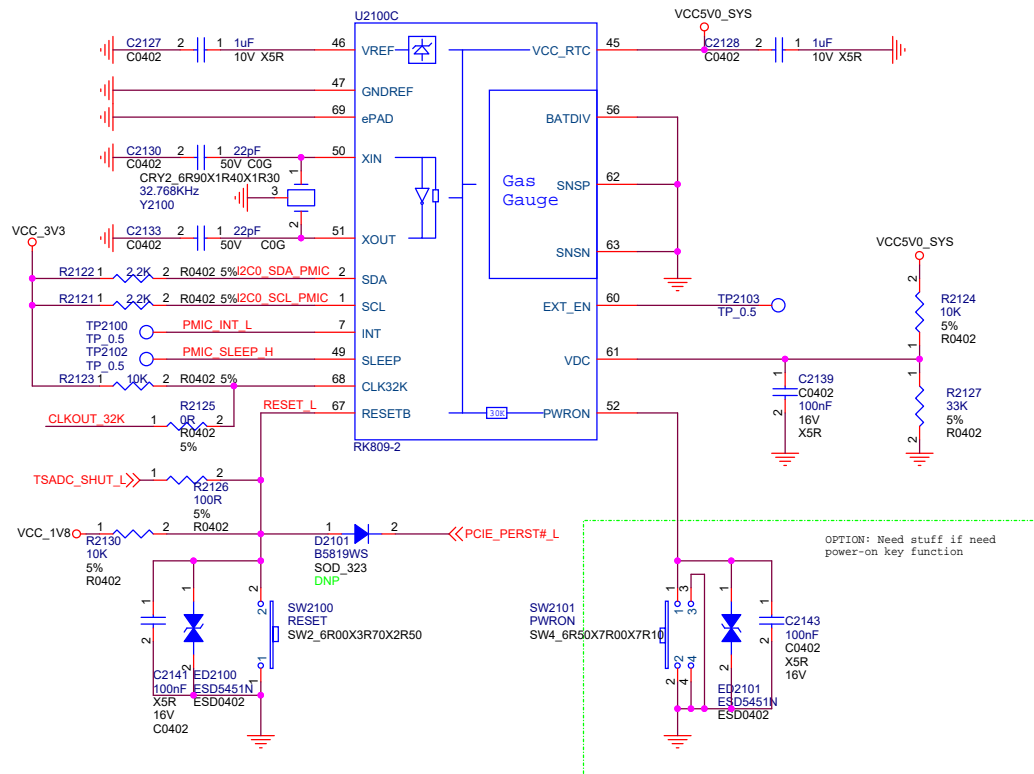


## PMIC RK809-2 LDO

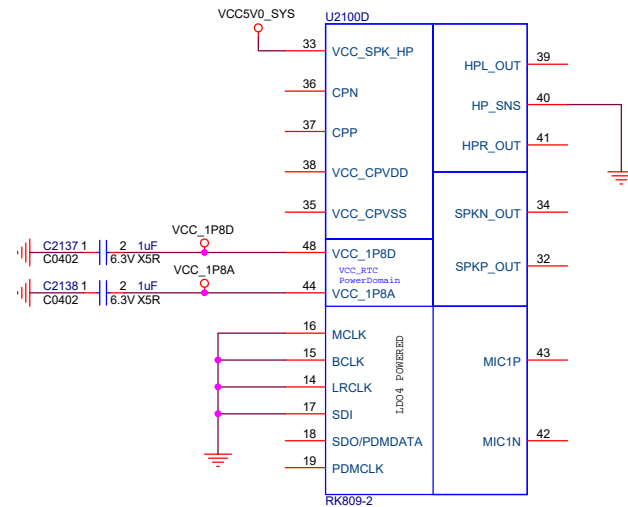


## PMIC RK809-2 Managerment

<< CLKOUT\_32K  
 << I2C0\_SDA\_PMIC  
 << I2C0\_SCL\_PMIC  
 << PMIC\_INT\_L  
 << PMIC\_SLEEP\_H  
 << RESET\_L

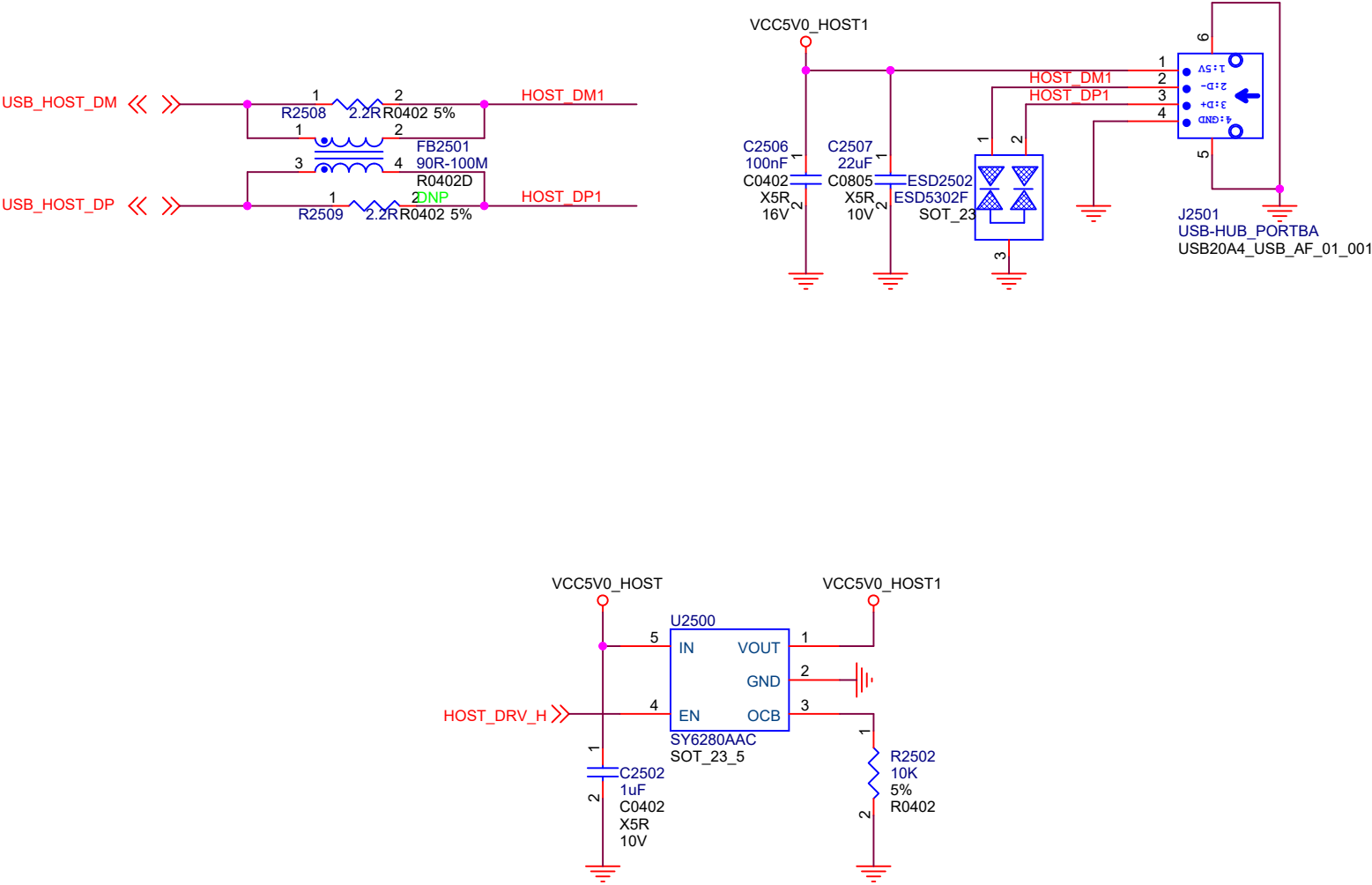


## PMIC RK809-2 CODEC

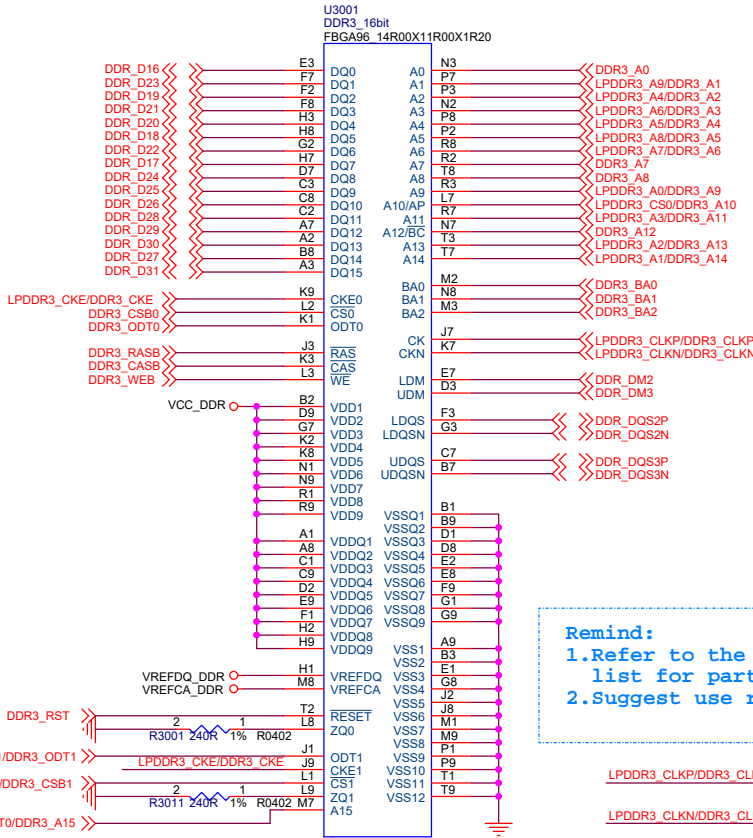
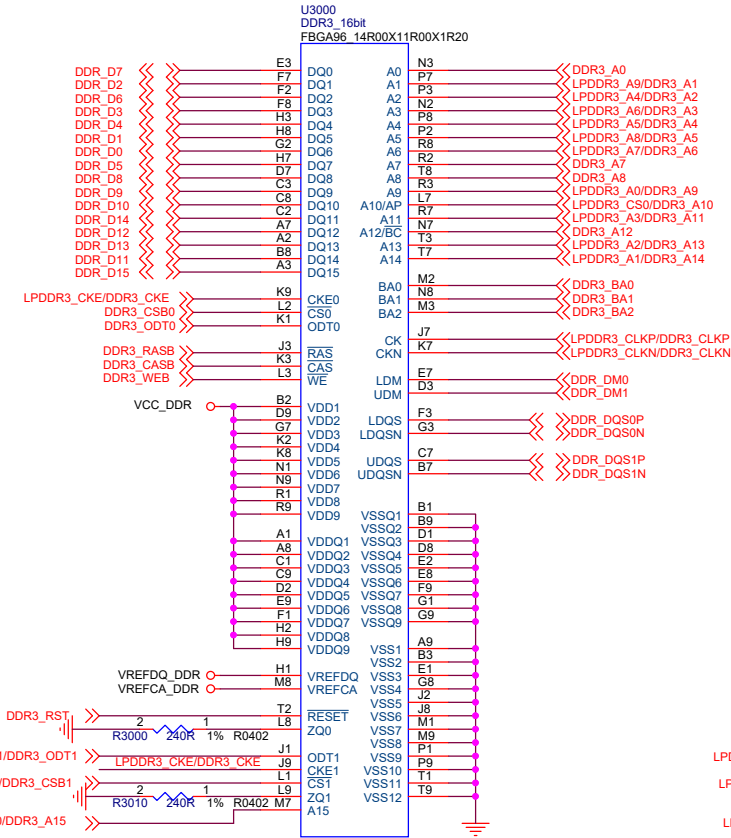


USB20 HOST

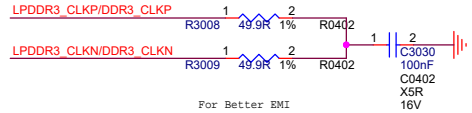
Option



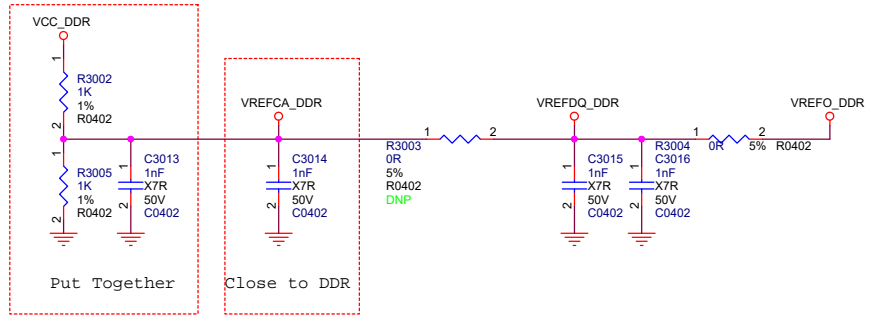
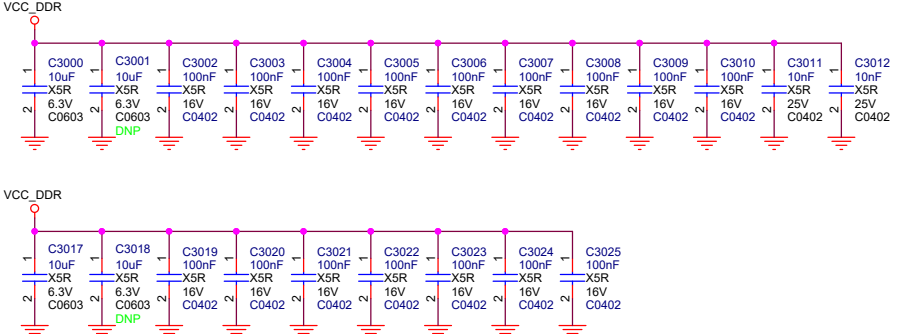
DDR3/DDR3L 2x16bit



Remind:  
1.Refer to the latest ddr support list for parts selection.  
2.Suggest use rk ddr template.

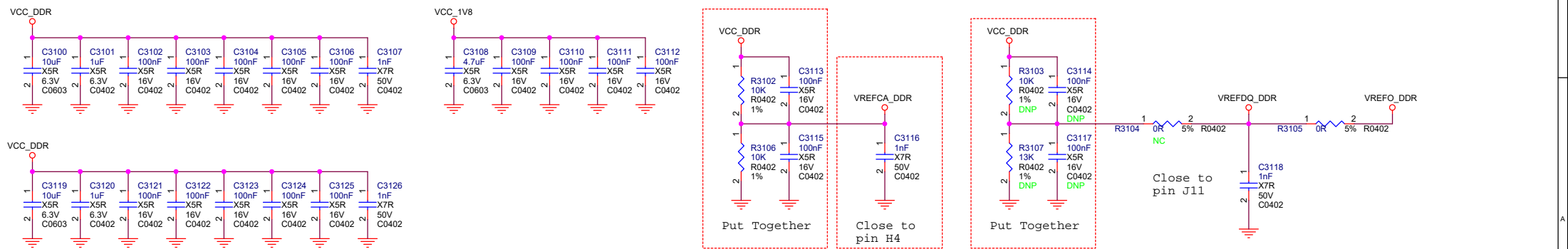
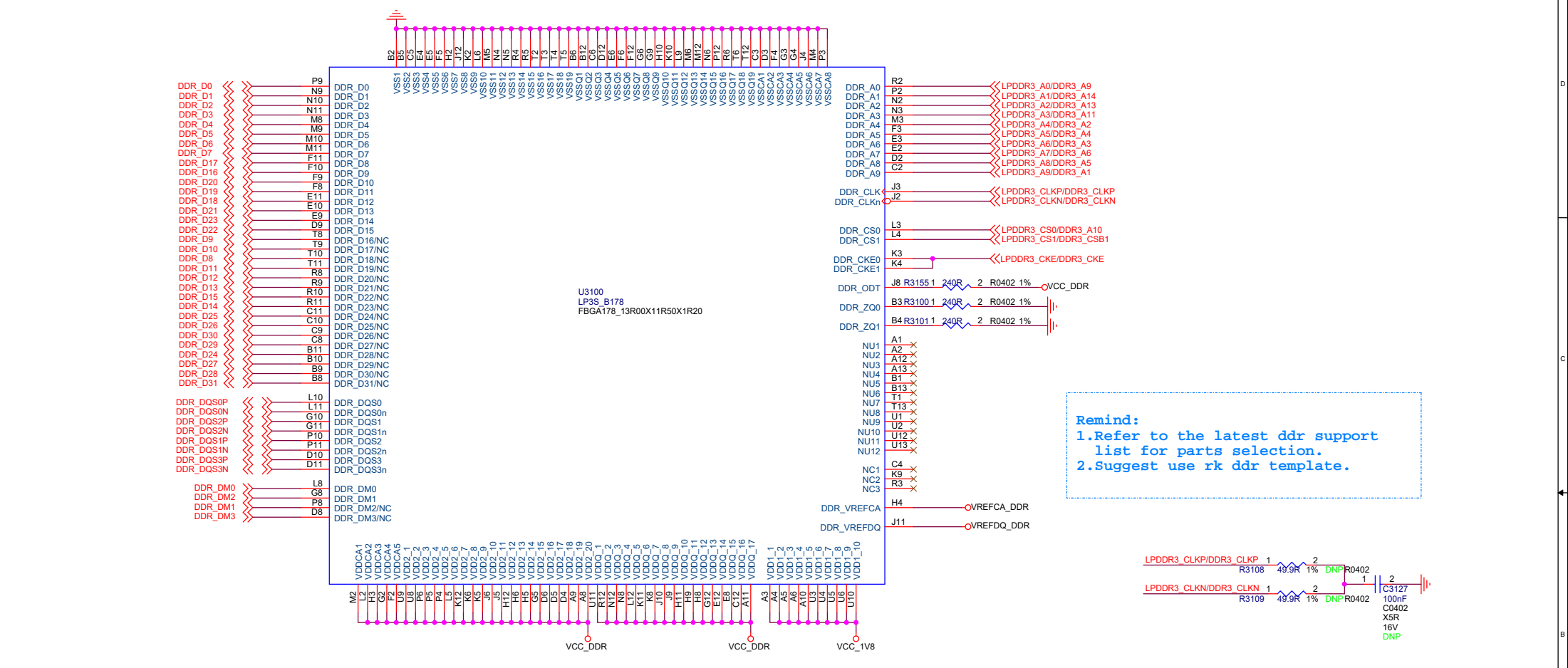


Note:  
All the Power filter capacitors should be placed close to the power pins of DDR3

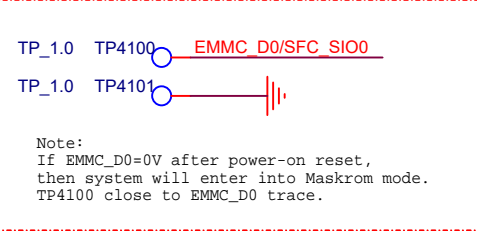
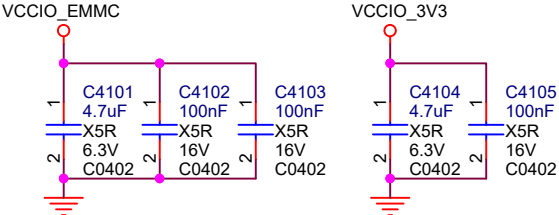
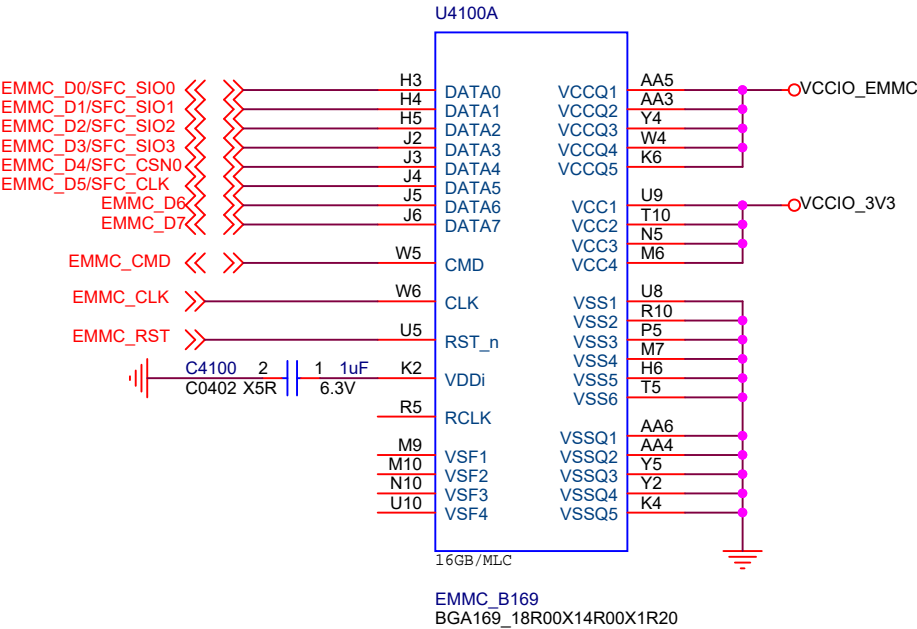
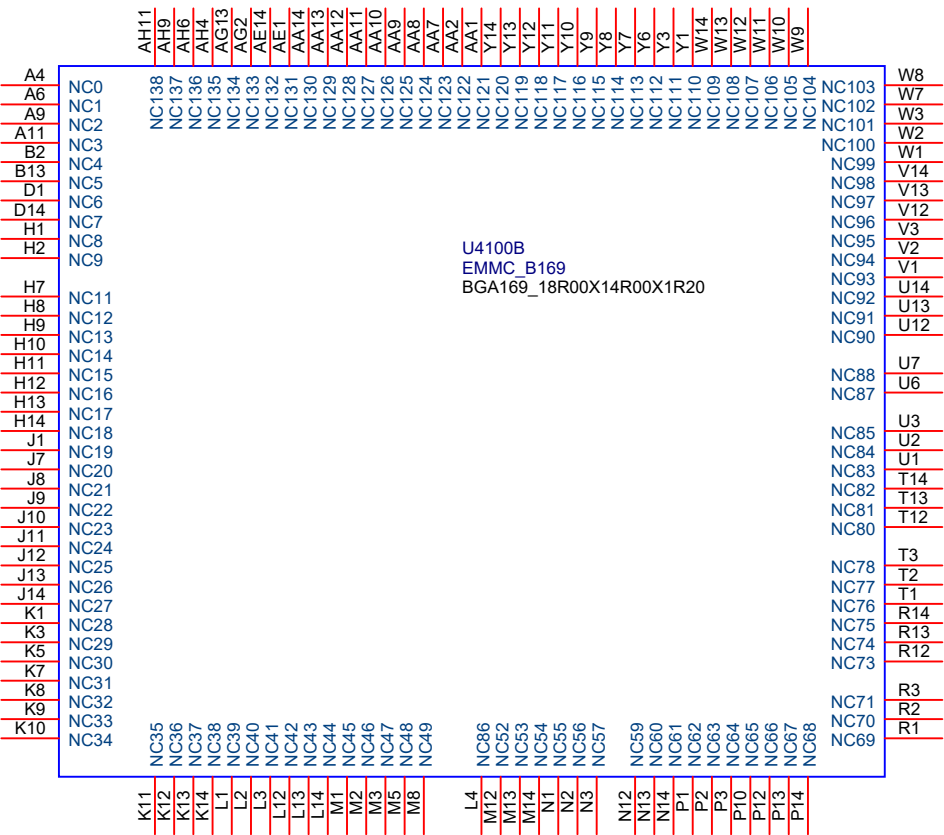


R3004=NC,R3003 need stuff.  
R3004=0R,R3003=DNP.(Default)  
Vrefo\_DDR POWER will shut off  
if VDD\_LOG power shut off.


LPDDR3 1x32bit



eMMC



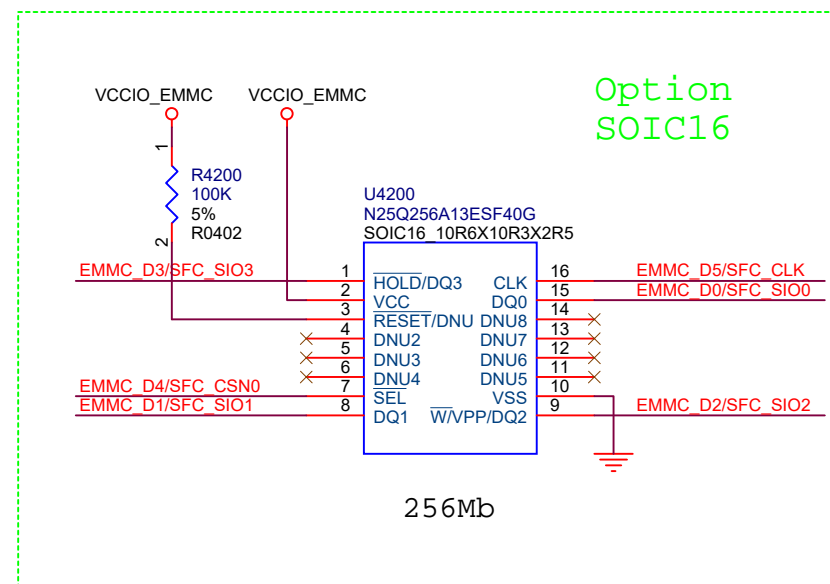
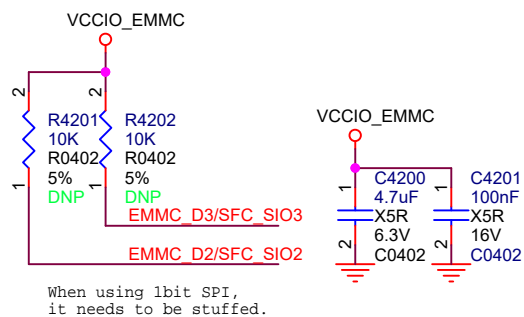
Remind: Refer to the latest eMMC Support List for parts selection.

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File:	41.EMMC		
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<< >>EMMC\_D0/SFC\_SIO0  
<< >>EMMC\_D1/SFC\_SIO1  
<< >>EMMC\_D2/SFC\_SIO2  
<< >>EMMC\_D3/SFC\_SIO3  
<< >>EMMC\_D4/SFC\_CSN0  
<< >>EMMC\_D5/SFC\_CLK

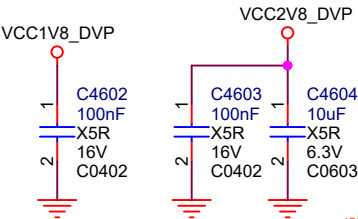
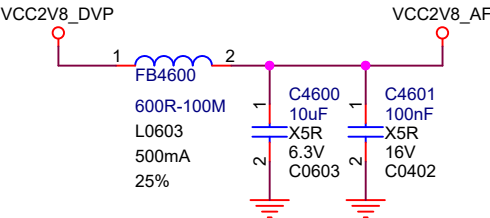
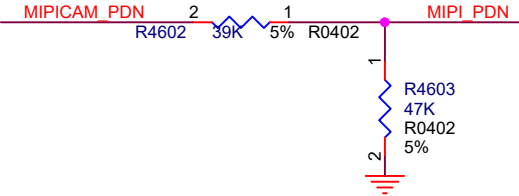
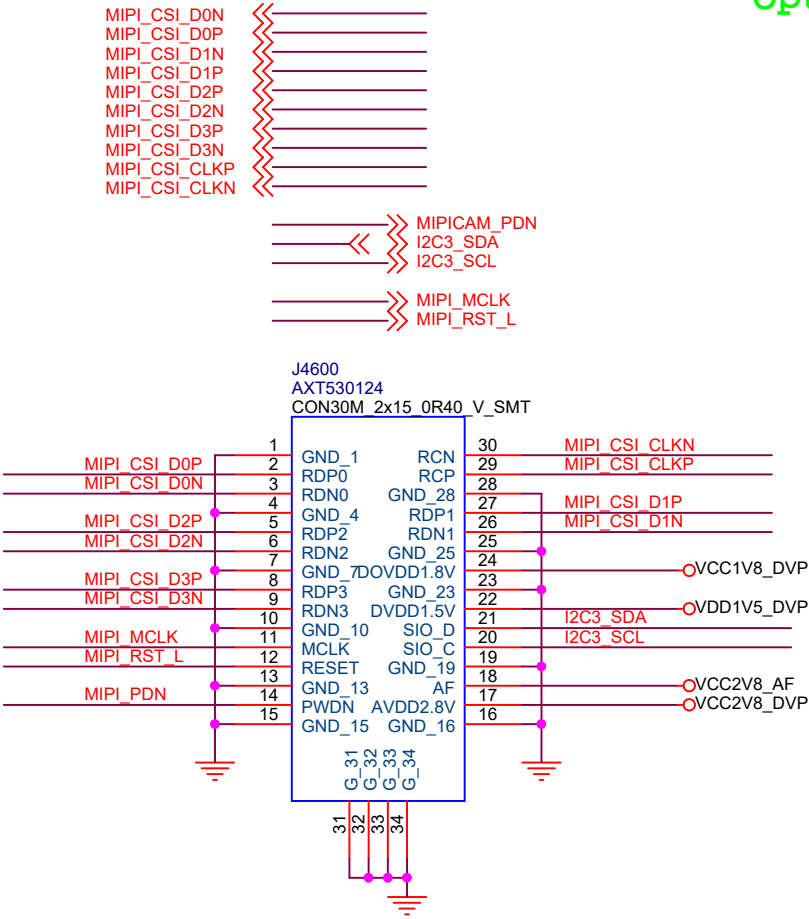
# SPI NOR Flash

Reserved for minimal system.

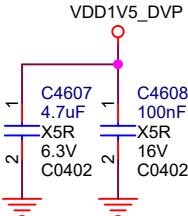
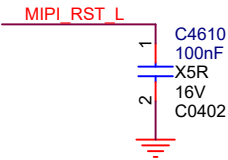
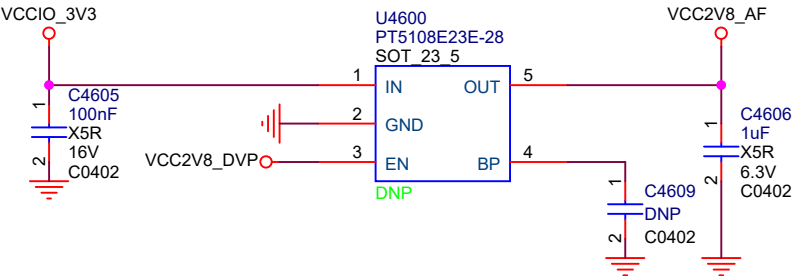



MIPI Camera

Option



NOTE:  
Adopt connection mode option2,  
mipi camera can't be used.

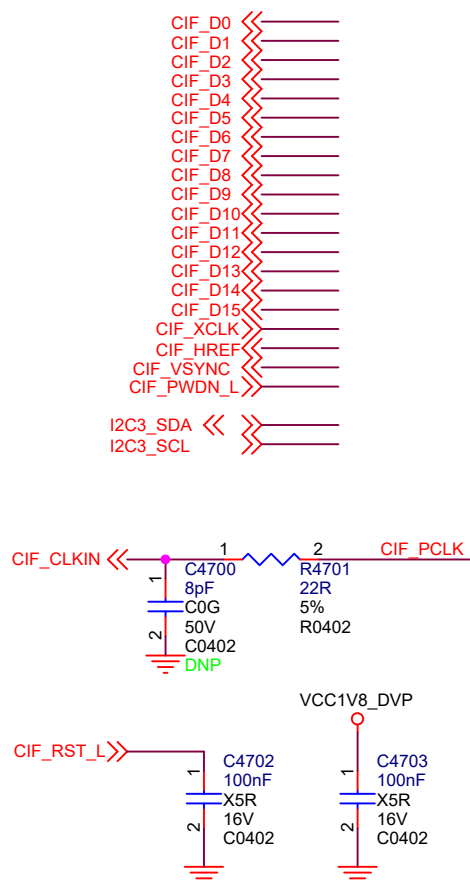


 瑞芯微电子		Fuzhou Rockchip Electronics	
Project:	RK1808_REF_V10		
File:	46.MIPI Camera		
Date:	Thursday, January 03, 2019	Rev:	V1.0
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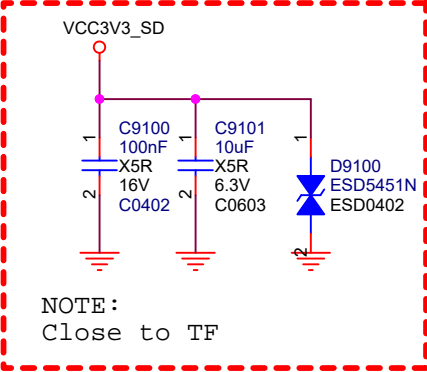
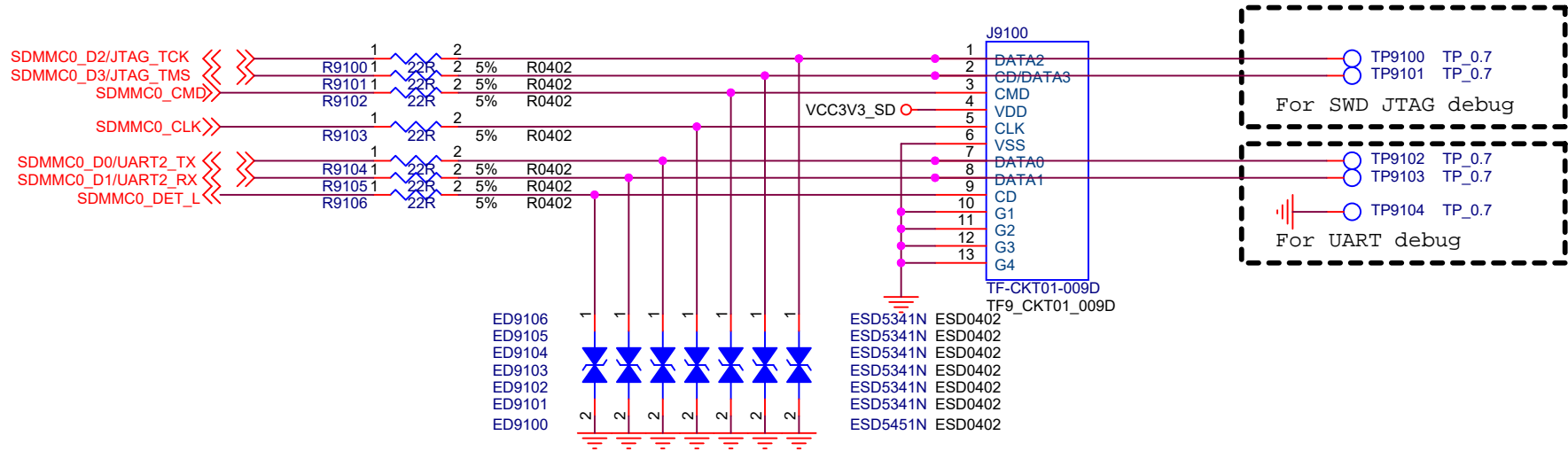



SENSOR: IMX323/ AR0230

## CIF CAM OPTION

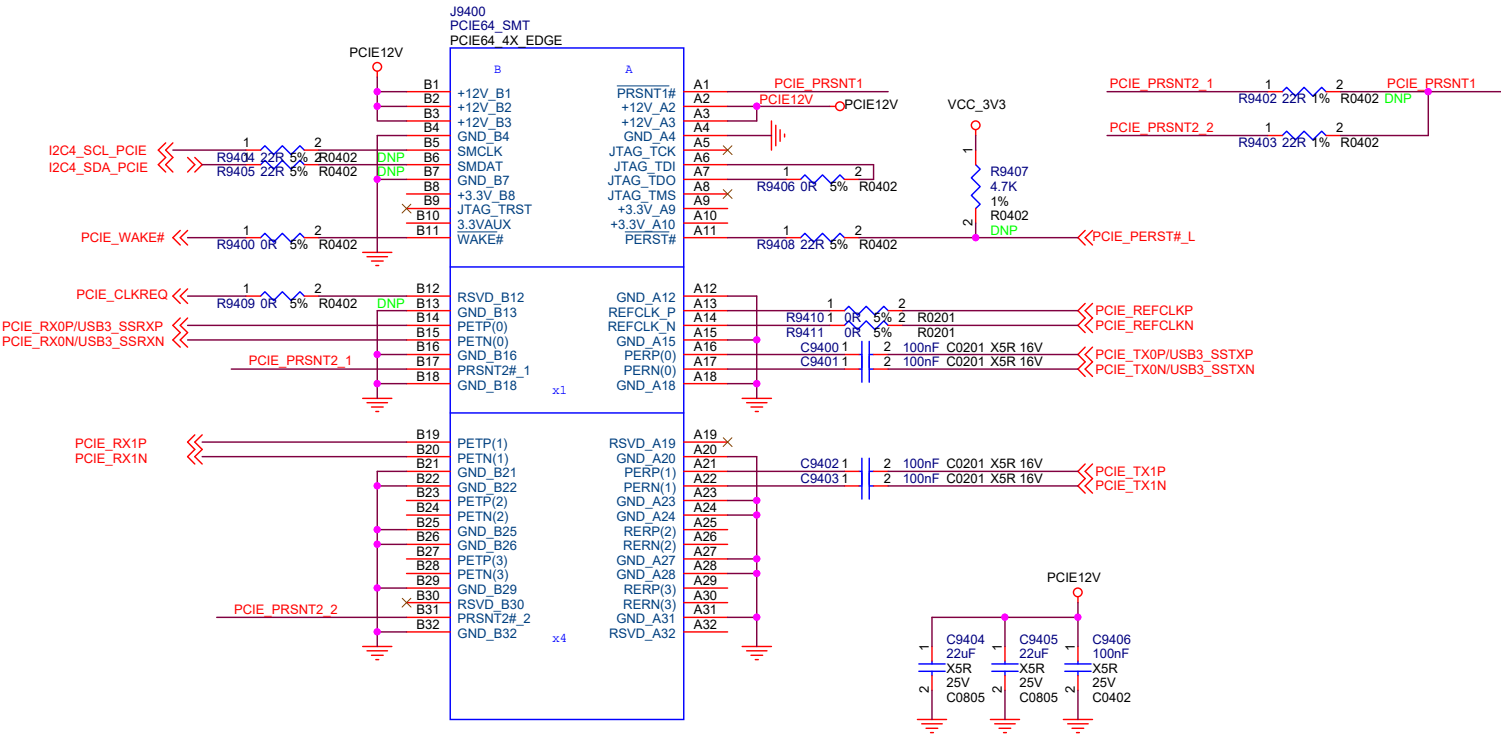


TF Card



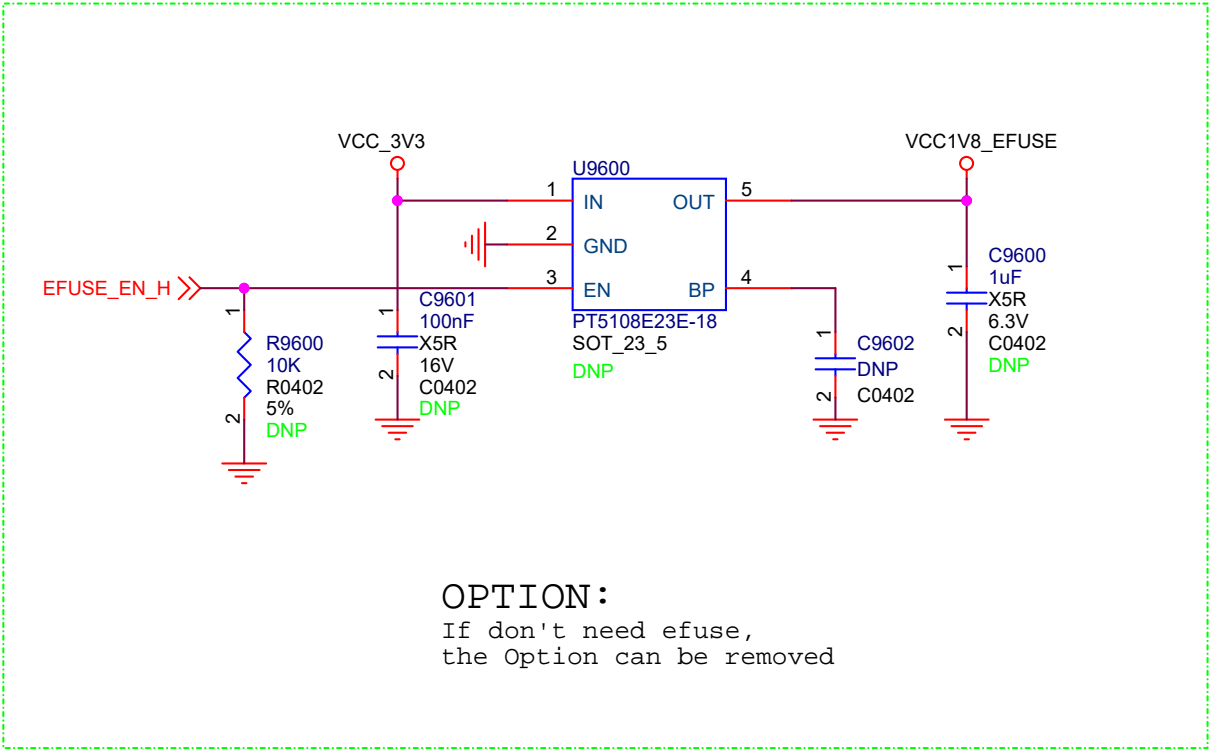
 瑞芯微电子		Fuzhou Rockchip Electronics	
Project:	RK1808_REF_V10		
File:	91.TF Card		
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PCIE EP CONNECTOR OPTION3



Efuse

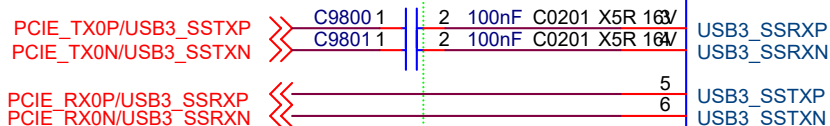
OPTION



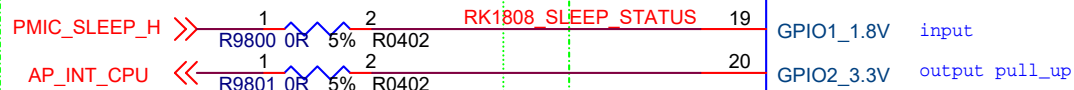
OPTION:  
If don't need efuse,  
the Option can be removed

<div><div><div><div><div><div></div></div><div><div>Rockchip</div></div></div><div><div>瑞芯微电子</div></div></div><div>Fuzhou Rockchip Electronics</div></div></div>			
Project:	RK1808_REF_V10		
File:	96.EFUSE		
Date:	Thursday, January 03, 2019	Rev:	V1.0
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## CONNECTION MODE OPTION1



OTG\_DP  
 OTG\_DM



MIPI\_CSI\_D0N  
 MIPI\_CSI\_D0P

MIPI\_CSI\_D1N  
 MIPI\_CSI\_D1P

MIPI\_CSI\_D2N  
 MIPI\_CSI\_D2P

MIPI\_CSI\_D3N  
 MIPI\_CSI\_D3P

MIPI\_CSI\_CLKN  
 MIPI\_CSI\_CLKP

## CONNECTION MODE OPTION2

AP

J9600

USB3\_SSRXP  
 USB3\_SSRXN

USB3\_SSTXP  
 USB3\_SSTXN

DP  
 DM

GPIO1\_1.8V input

GPIO2\_3.3V output pull\_up

MIPI\_TX\_D0N  
 MIPI\_TX\_D0P

MIPI\_TX\_D1N  
 MIPI\_TX\_D1P

MIPI\_TX\_D2N  
 MIPI\_TX\_D2P

MIPI\_TX\_D3N  
 MIPI\_TX\_D3P

MIPI\_TX\_CLKN  
 MIPI\_TX\_CLKP

GND1

AP CONNECTOR

MIPI\_RX\_D0N  
 MIPI\_RX\_D0P

MIPI\_RX\_D1N  
 MIPI\_RX\_D1P

MIPI\_RX\_D2N  
 MIPI\_RX\_D2P

MIPI\_RX\_D3N  
 MIPI\_RX\_D3P

MIPI\_RX\_CLKN  
 MIPI\_RX\_CLKP

GND2

MIPI\_DSI\_D0N  
 MIPI\_DSI\_D0P

MIPI\_DSI\_D1N  
 MIPI\_DSI\_D1P

MIPI\_DSI\_D2N  
 MIPI\_DSI\_D2P

MIPI\_DSI\_D3N  
 MIPI\_DSI\_D3P

MIPI\_DSI\_CLKN  
 MIPI\_DSI\_CLKP

## NOTE:

### CONNECTION MODE:

- 1:USB20+USB30+GPIOX2(option1) Default
- 2.USB20+MIPI+GPIOX2(option2)
- 3.USB20+PCIE+GPIO(Option3)

USB20 OTG for down load,  
 USB30\MIPI\PCIE for transfer  
 large data; Gpio for detect sleep  
 status and int generation detect.

**Rockchip**  
 瑞芯微电子

Fuzhou Rockchip Electronics

**Project:** RK1808\_REF\_V10

**File:** 98.AP CONNECTOR

**Date:** Thursday, January 03, 2019

**Rev:** V1.0

**Designed by:** Rzfi

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